WHAT IS CLAIMED IS:

1. A ferroelectric memory device comprising:

at least two bottom electrode patterns formed on a semiconductor substrate;

a first ferroelectric layer on the semiconductor substrate between the bottom electrode patterns, wherein a top surface of the first ferroelectric layer is substantially aligned with top surfaces of the bottom electrode patterns; and

a second ferroelectric layer on the top surface of the bottom electrode patterns and the top surface of the first ferroelectric layer.

2. The ferroelectric memory device of Claim 1, further comprising a seed layer between the first ferroelectric layer and the semiconductor substrate.

3. The ferroelectric memory device of Claim 2, wherein the seed layer comprises at least one of TiO_2 and $SrRuO_3$.

4. The ferroelectric memory device of Claim 2, further comprising a planarization assistant layer between the seed layer and the semiconductor substrate.

5. The ferroelectric memory device of Claim 4, wherein the seed layer is a reaction barrier layer which inhibits reaction between the first ferroelectric layer and the planarization assistant layer.

6. The ferroelectric memory device of Claim 4, wherein:

the planarization assistant layer comprises silicon oxide; and

the first ferroelectric layer comprises $Pb(Zi, Ti)O_3$ [PZT].

7. A ferroelectric memory device comprising:

at least two bottom electrode patterns formed on a semiconductor substrate;

a seed layer on the semiconductor substrate between the bottom electrode patterns;

a first ferroelectric layer on the seed layer; and

a second ferroelectric layer on the top surface of the bottom electrode patterns and a top surface of the first ferroelectric layer.

8. The ferroelectric memory device of Claim 7, further comprising a planarization assistant layer between the seed layer and the semiconductor substrate.

9. The ferroelectric memory device of Claim 8, wherein the seed layer is a reaction barrier layer which inhibits reaction between the first ferroelectric layer and the planarization assistant layer.

10. The ferroelectric memory device of Claim 8, wherein:
the planarization assistant layer comprises silicon oxide; and
the first ferroelectric layer comprises $Pb(Zi, Ti)O_3$ [PZT].

11. The ferroelectric memory device of Claim 7, wherein the seed layer comprises at least one of TiO_2 and $SrRuO_3$.

12. The ferroelectric memory device of Claim 7, further comprising an oxidation barrier layer between the seed layer and the semiconductor substrate.

13. The ferroelectric memory device of Claim 12, wherein the oxidation barrier layer comprises at least one of Al_2O_3, TiO_2, ZrO_2, and CeO_2.

14. The ferroelectric memory device of Claim 7, further comprising an adhesion assistant layer pattern between the semiconductor substrate and the bottom electrode patterns.

15. The ferroelectric memory device of Claim 14, wherein the adhesion assistant layer pattern comprises at least one of titanium, tantalum, iridium, ruthenium, tungsten, titanium nitride, tantalum nitride, iridium nitride, ruthenium nitride, tungsten nitride, titanium silicide, tantalum silicide, iridium silicide, ruthenium silicide and tungsten silicide.

16. The ferroelectric memory device of Claim 7, wherein the first ferroelectric layer comprises at least one of $Pb(Zr,Ti)O_3$ [PZT], $PbTiO_3$, $PbZrO_3$, La-doped PZT [$(Pb, La)(Zr, Ti)O_3$], PbO, $SrTiO_3$, $BaTiO_3$, $(Ba,Sr)TiO_3$ [BST],

$SrBi_2Ta_2O_9$ [SBT], and $Bi_4Ti_3O_{12}$.

17. The ferroelectric memory device of Claim 7, wherein the bottom electrode patterns comprise at least one of platinum, ruthenium, iridium, rhodium, osmium, palladium, platinum oxide, ruthenium oxide, iridium oxide, rhodium oxide, osmium oxide, and palladium oxide.

18. A ferroelectric memory device, comprising:

an interlayer insulation layer on a semiconductor substrate;

at least two contact plugs on the semiconductor substrate and extending through the interlayer insulation layer;

at least two bottom electrode patterns on the interlayer insulation layer, each of the bottom electrode patterns electrically connected with a different respective one of the two contact plugs;

a seed layer on the interlayer insulation layer between the bottom electrode patterns;

a first ferroelectric layer on the seed layer opposite to the interlayer insulation layer, wherein a top surface of the first ferroelectric layer is substantially aligned with top surfaces of the bottom electrode patterns; and

a second ferroelectric layer on the top surface of the bottom electrode patterns and the top surface of the first ferroelectric layer.

19. A ferroelectric memory device of Claim 18, further comprising a common capacitor top electrode pattern on the second ferroelectric layer.

20. A ferroelectric memory device of Claim 18, further comprising:

a planarization assistant layer between the seed layer and the interlayer insulation layer; and

an oxidation barrier layer between the planarization assistant layer and the interlayer insulation layer.